

<b>Notice of References Cited</b>	Application/Control No. 09/931,131	Applicant(s)/Patent Under Reexamination KIM ET AL.	
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**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,389,374	05-2002	Jain et al.	703/2
	B	US-6,212,669	04-2001	Jain, Jawahar	716/7
	C	US-6,086,626	07-2000	Jain et al.	716/5
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Ravi, K. et al., "Approximating and decomposition of binary decision diagrams", 6/1998, ACM, pgs. 1-6.
	V	Yang et al., "BDS: A BDD-based logic optimization system", 6/2000, ACM, pgs. 92-97.
	W	Wang et al., "Restructuring binary decision diagrams based on functional equivalence", 2/1993, IEEE, pgs. 261-265.
	X	Chakrabarti et al., "Synthesis of symmetric functions for path-delay fault testability", 9/2000, IEEE, pgs. 1076-1081.

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Touba et al., "RP-Syn: synthesis of random pattern testable circuits with test point insertion", 8/1999, IEEE, pgs. 1202-1213.
	V	
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.